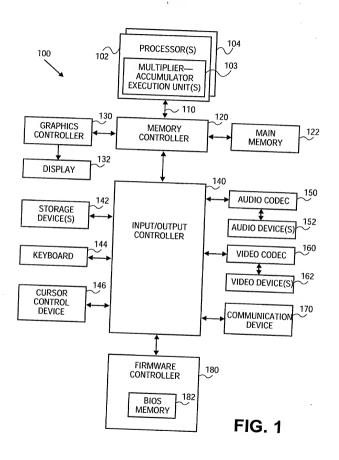
# TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062.143



#### TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062.143

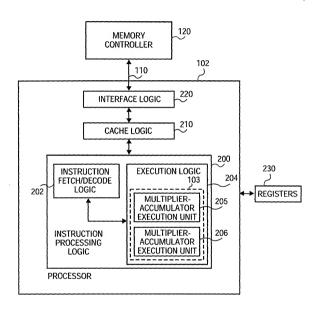
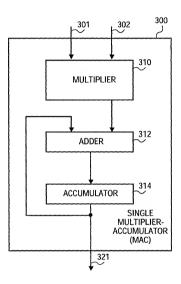
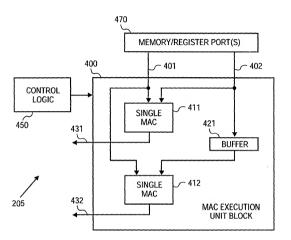


FIG. 2



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FIG. 3



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FIG. 4

#### TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062 143

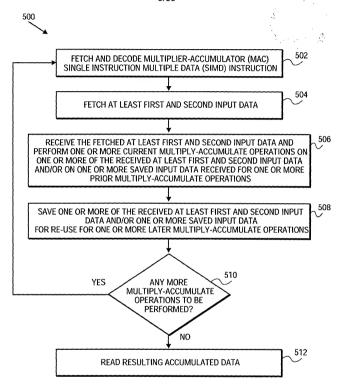


FIG. 5

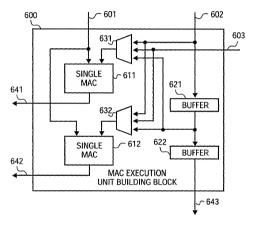


FIG. 6

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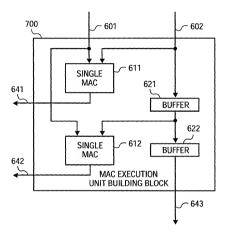


FIG. 7

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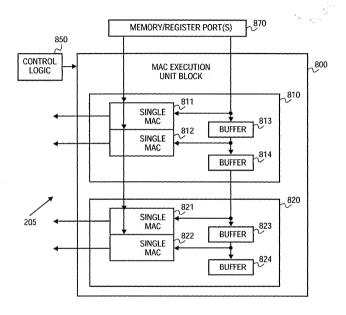


FIG. 8

# TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062,143

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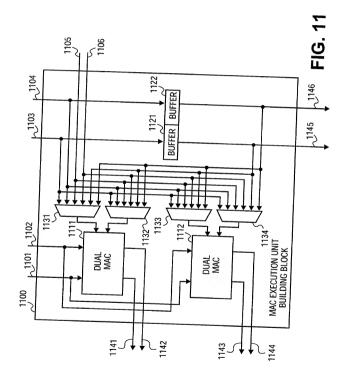
	Computation Cycle N	n Cycle N	Computatic	Computation Cycle N+1	Computation	Computation Cycle N+2
MAC	1st MAC Input	2nd MAC Input	1st MAC Input	2nd MAC Input	1st MAC Input	2nd MAC Input
811: y(3)	c(31)	x(-28)	c(30)	x(-27)	c(29)	x(-26)
812: y(2)	c(31)	x(-29)	c(30)	x(-28)	c(29)	x(-27)
821: y(1)	c(31)	x(-30)	c(30)	x(-29)	c(29)	x(-28)
822: y(0)	(18)	x(-31)	(30)	(0E-)x	c(29)	(-53)

FIG. 9

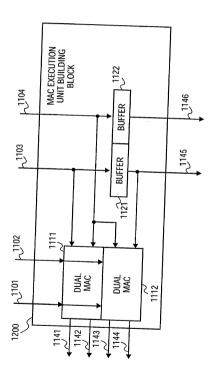
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FIG. 10

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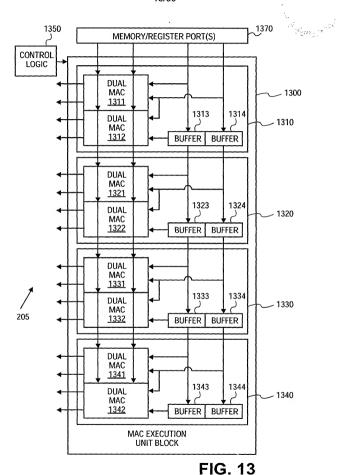


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TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062.143



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	^		4th MAC	Innit	150	x(-20)	(-12)	x(-21)		x(-22)		x(-23)	(20)	(+7-)x	x(-25)	1 50	x(-26)	(2)	x(-27)
	Computation Cycle N+2	200	2nd MAC	Inort		c(27)		C(27)		C(27)		c(27)	(10)	(/7)	(77)	į	c(27)		c(27)
	omputation		3rd MAC	Input		x(-19)	100	(07-)x	(20)	(17-)x	100/1	(77-)x	x(-23)	W 20)	x(-24)		x(-25)		(97-)x
Ľ	_		1st MAC	Input	(00)	(4Z)	(30)	د(ح٥)	(30)	(20)	(30)	د(20)	(96)	(61)	C(56)	1000	(97)	(30)0	د(20)
		441. 0 000	4th IMAC	Indu	(00)	(77-)v	v(-23)	V(27)	(VC-)X	W(-2-1)	x(-25)	(57)	x(-26)	(10)	(/Z-)x	(00 /^	(07-)v	(00)	(C7_)v
Color M. 1	oyere N+1	ONA NAC	ZIIU IVIAC	II DOI	(00)	(67)	6	(2)	6	2	600		(67) (2)	(00)	(62)	(00)	(53)	(00)	0(40)
Commitation Orch N. 1	Damadi	3rd MAC	Thirt in	100	x(-21)		(77-)X		X-73		X(-24)	(20)	(C7-)x	(30)	v(-20)	x(-27)		(8/-)X	
Ē		1st MAC	hout	1	c(28)	(00)	(87 (28)	(00)	(87)	(00)0	(07)	(00)	(20)	(80)	(00)	(87)	(00)	(87 (28)	
		4th MAC	Indu		x(-24)	V 2E)	(CZ-)V	(36)	(05-)v	(LC)^	(/Z/)	(2C-)x	(27)	x(-29)	100	v(-30)	16/2	(اد)	1
n Cycle N	1st MAC 3rd MAC 2rd MAC 2rd MAC 1st MAC 1st MAC 3rd MAC 2rd MAC 1st MAC 3rd MA	Input	100	(3)	((31)	(10)	(131)	(10)	(31)	(10)	c(31)		C(31)	(121)	23	C/21)			
omputatic		Input	(00)	(cz-)v	x(-24)	-	x(-25)		x(-26)		x(-27)	100/	(87-)x	(bC-)x	(27)	x(-30)			
	10+1400	SLIMAC	Input	(30)	(20)	(30)		(30)		(05)	100	(30)	(00)	(00)	c(30)		c(30)		
	MAC	2		1311· v(7)	(1)	1312: y(6)	1221	(2)(:)(2)	1222	1322: )(4)	1001(0)	1331: 3(3)	1332. (7)	100E: J(E)	1341: y(1)	40.00	1342: y(0)		

FIG. 14

#### TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062,143

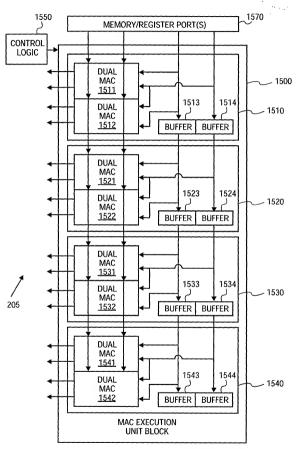


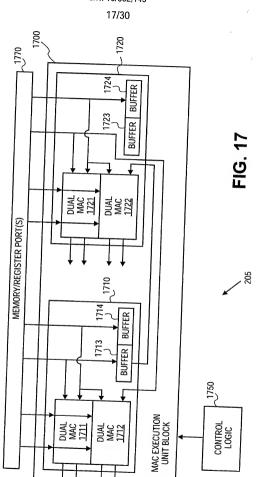
FIG. 15

## TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062,143

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	4th MAC Input	x(-26)i	x(-26)r	x(-27)i	x(-27)r	x(-28)i	x(-28)r	x(-29)i	x(-29)r
Cycle N+2	2nd MAC Input	c(23)i	c(29)i	c(29)i	c(29)i	c(23)i	c(29)i	c(29)i	c(29)i
Computation Cycle N+2	Input	x(-26)r	x(-26)i	x(-27)r	x(-27)i	x(-28)r	x(-28)i	x(-29)r	x(-29)i
පි	1st MAC Input	c(29)r							
	4th MAC Input	x(-27)i	x(-27)r	x(-28)i	x(-28)r	x(-29)i	x(-29)r	x(-30)i	x(-30)r
Computation Cycle N+1	2nd MAC Input	1	c(30)i						
mputation	3rd MAC	x(-27)r	x(-27)i	x(-28)r	x(-28)i	x(-29)r	x(-29)i	x(-30)r	x(-30)i
8	1st MAC Input	,	c(30)r						
	4th MAC Input		x(-28)r	x(-29)i	x(-29)r	x(-30)i	x(-30)r	x(-31)i	x(-31)r
on Cycle N	2nd MAC Input		c(31)i						
Computation Cycle N	3rd MAC Input	x(-28)r	x(-28)i	x(-29)r	x(-29)i	x(-30)r	x(-30)i	x(-31)r	x(-31)i
	1st MAC Input	c(31)r							
	MAC	1511: y(3)r	1512: y(3)i	1521: y(2)r	1522: y(2)i	1531: y(1)r	1532: y(1)i	1541: y(0)r	1542: y(0)i

FIG. 16

# TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062,143



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_	()	$\neg$				(2)	_		_		()	_		
	4th MA(	Input	x(-30)	x(-31)		4th MA(	Input	x(-26)	x(-27)		4th MA(	Input	x(-22)	x(-23)
	1st MAC   3rd MAC   2nd MAC   4th MAC	Input	(15)2	c(31)		1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(27)	c(27)		1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(23)	c(23)
	3rd MAC	Input	(6Z-)x	x(-30)		3rd MAC	Input	x(-25)	x(-26)		3rd MAC	Input	x(-21)	x(-22)
	1st MAC	Input	c(30)	c(30)		1st MAC	Input	c(26)	c(26)		1st MAC	Input	c(22)	c(22)
Computation Cycle N	MAC		1721: y(1)	1722: y(0)	Computation Cycle N+1	MAC		1721: y(1)	1722: y(0)	Computation Cycle N+2	MAC		1721: y(1)	1722: y(0)
Computa	4th MAC	Input	x(-28)	x(-29)	Computati	4th MAC	Input	x(-24)	x(-25)	Computati	4th MAC	Input	x(-20)	x(-21)
	1st MAC   3rd MAC   2nd MAC   4th MAC	Input	(6Z)0	c(29)		1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(25)	c(25)		1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(21)	c(21)
	3rd MAC	Input	(2-)x	x(-28)		3rd MAC	Input	x(-23)	x(-24)		3rd MAC	Input	x(-19)	x(-20)
	1st MAC	Input	c(28)	c(28)		1st MAC	Input	c(24)	c(24)		1st MAC	Input	c(20)	c(20)
	MAC		1711: y(1)	1712: y(0)		MAC		1711: y(1)	1712: y(0)		MAC		1711: y(1)	1712: y(0)

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### TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062,143

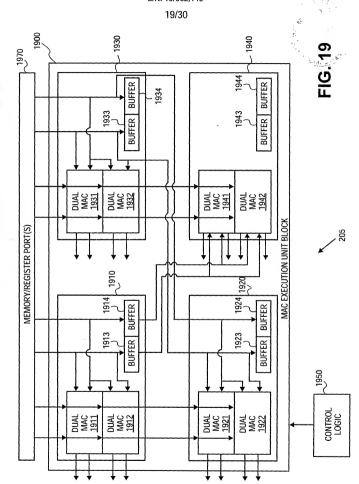
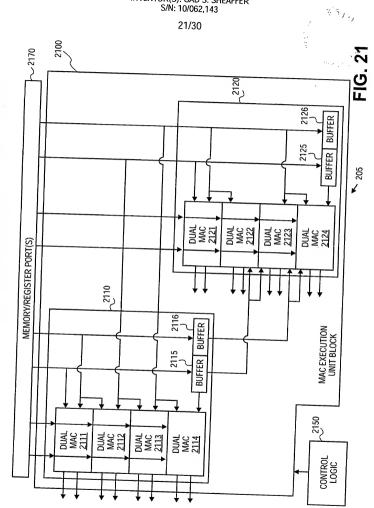


FIG. 20

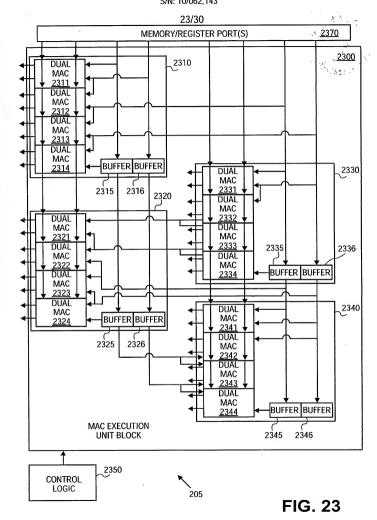
	4th MAC	Input	x(-30)i	x(-30)r	x(-31)i	x(-31)r		4th MAC	Input	x(-28)i	x(-28)r	x(-29)i	x(-29)r		4th MAC	Input	x(-26)i	x(-26)r	x(-27)i	x(-27)r
	2nd MAC	Input	c(31)i	c(31)i	c(31)i	c(31)i		3rd MAC 2nd MAC 4th MAC	Input	c(29)i	c(29)i	c(29)i	c(29)i		3rd MAC 2nd MAC 4th MAC	Input	c(27)i	c(27)i	c(27)i	c(27)i
	3rd MAC 2nd MAC 4th MAC	Input	x(-30)r	x(-30)i	x(-31)r	x(-31)i			Input	x(-28)r	x(-28)i	x(-29)r	x(-29)i			Input	x(-26)r	x(-26)i	x(-27)r	x(-27)i
	1st MAC	Input	c(31)r	c(31)r	c(31)r	c(31)r		1st MAC	Input	c(29)r	c(29)r	c(29)r	c(29)r		1st MAC	Input	c(27)r	c(27)r	c(27)r	c(27)r
Computation Cycle N	MAC		1931: y(1)r	1932: y(1)i	1941: y(0)r	1942: y(0)i	Computation Cycle N+1	MAC		1931: y(1)r	1932: y(1)i	1941: y(0)r	1942: y(0)i	Computation Cycle N+2	MAC		1931: y(1)r	1932: y(1)i	1941: y(0)r	1942: y(0)i
Computa	4th MAC	Input	x(-29)i	x(-29)r	x(-30)i	x(-30)r	Computati	4th MAC	Input	x(-27)i	x(-27)r	x(-28)i	x(-28)r	Computati	4th MAC	Input	x(-25)i	x(-25)r	x(-26)i	x(-26)r
	1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(30)i	c(30)i	c(30)i	c(30)i		1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(28)i	c(28)i	c(28)i	c(28)i		3rd MAC 2nd MAC 4th MAC	Input	c(26)i	c(26)i	c(26)i	c(26)i
	3rd MAC	Input	x(-29)r	x(-29)i	x(-30)r	x(-30)i		3rd MAC	Input	x(-27)r	x(-27)i	x(-28)r	x(-28)i		3rd MAC	Input	x(-25)r	x(-25)i	x(-26)r	x(-26)i
	1st MAC	Input	c(30)r	c(30)r	c(30)r	c(30)r		1st MAC	Input	c(28)r	c(28)r	c(28)r	c(28)r		1st MAC	Input	c(26)r	c(26)r	c(26)r	c(26)r
	MAC		1911: y(1)r	1912: y(1)i	1921: y(0)r	1922: y(0)i		MAC		1911: y(1)r	1912: y(1)i	1921: y(0)r	1922: y(0)i		MAC		1911: y(1)r	1912: y(1)i	1921: y(0)r	1922: y(0)i



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	4th MAC	Input	x(-28)	x(-29)	x(-30)	x(-31)		4th MAC	Indu	x(-24)	x(-25)	x(-26)	x(-27)		4th MAC	Input	x(-20)	x(-21)	x(-22)	x(-23)
	1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(31)	c(31)	c(31)	c(31)		1st MAC   3rd MAC   2nd MAC 4th MAC	Indut	c(27)	c(27)	c(27)	c(27)		3rd MAC 2nd MAC 4th MAC	Input	c(23)	c(23)	c(23)	c(23)
	3rd MAC	Input	x(-27)	x(-28)	x(-29)	x(-30)		3rd MAC	Input	x(-23)	x(-24)	x(-25)	x(-26)		3rd MAC	Input	x(-19)	x(-20)	x(-21)	x(-22)
	1st MAC	Input	c(30)	c(30)	c(30)	c(30)		1st MAC	Input	c(26)	c(26)	c(26)	c(26)		1st MAC	Input	c(22)	c(22)	c(22)	c(22)
Computation Cycle N	MAC		2121: y(3)	2122: y(2)	2123: y(1)	2124: y(0)	Computation Cycle N+1	MAC		2121: y(3)	2122: y(2)	2123: y(1)	2124: y(0)	Computation Cycle N+2	MAC		2121: y(3)	2122: y(2)	2123: y(1)	2124: y(0)
Computat	4th MAC	Input	x(-26)	x(-27)	x(-28)	x(-29)	Computation	4th MAC	Input	x(-22)	x(-23)	x(-24)	x(-25)	Computati	4th MAC	Input	(81-)x	(-19)	x(-20)	x(-21)
	1st MAC   3rd MAC   2nd MAC   4th MAC	Indut	c(29)	c(29)	c(29)	c(29)		3rd MAC 2nd MAC 4th MAC	Input	c(25)	c(25)	c(25)	c(25)		1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(21)	c(21)	c(21)	c(21)
	3rd MAC	Input	x(-25)	x(-26)	x(-27)	x(-28)		3rd MAC	Input	x(-21)	x(-22)	x(-23)	x(-24)		3rd MAC	Inbr	x(-17)	x(-18)	(61-)x	x(-20)
	1st MAC	Input	c(28)	c(28)	c(28)	c(28)		1st MAC	Indu	c(24)	c(24)	c(24)	c(24)		1st MAC	Input	c(20)	c(20)	c(20)	c(20)
	MAC		2111: y(3)	2112: y(2)	2113: y(1)	2114: y(0)		MAC		2111: y(3)	2112: y(2)	2113: y(1)	2114: y(0)		MAC		2111: y(3)	2112: y(2)	2113: y(1)	2114: y(0)



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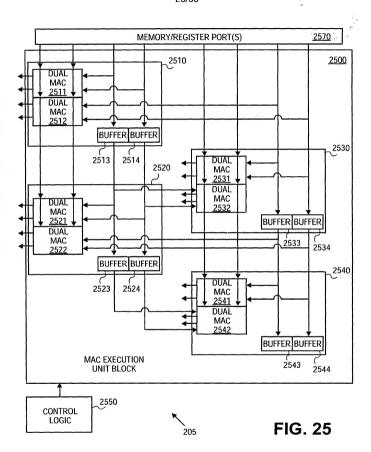
																			П	-	١
4th MAC	ın i	x(-24)	x(-25)	x(-26)	x(-27)	x(-28)	x(-29)	x(-30)	x(-31)		4th MAC	Input	x(-20)	x(-21)	x(-22)	x(-23)	x(-24)	x(-25)	x(-26)	x(-27)	7
1st MAC 3rd MAC 2rd MAC 4th MAC	ındı	c(31)		1st MAC 3rd MAC 2nd MAC	Input	c(27)	c(27)	c(27)	c(27)	c(27)	c(27)	c(27)	c(27)								
3rd MAC	III	x(-23)	x(-24)	x(-25)	x(-26)	x(-27)	x(-28)	x(-29)	x(-30)		3rd MAC	Input	x(-19)	x(-20)	x(-21)	x(-22)	x(-23)	x(-24)	x(-25)	x(-26)	
1st MAC	Indu	c(30)		1st MAC	Input	c(26)	c(26)	c(26)	c(26)	c(26)	c(26)	c(26)	c(26)								
MAC		2331: y(7)	2332: y(6)	2333: y(5)	2334: y(4)	2341: y(3)	2342: y(2)	2343: y(1)	2344: y(0)	Computation Cycle N+1	MAC		2331: y(7)	2332: y(6)	2333: y(5)	2334: y(4)	2341: y(3)	2342: y(2)	2343: y(1)	2344: y(0)	
4th MAC	Indu	x(-22)	x(-23)	x(-24)	x(-25)	x(-26)	x(-27)	x(-28)	x(-29)	Computation	4th MAC	Input	x(-18)	(6L-)x	x(-20)	x(-21)	x(-22)	x(-23)	x(-24)	x(-25)	
3rd MAC 2nd MAC 4th MAC	Input	(53)	c(29)		1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(25)	c(25)	c(25)	c(22)	c(25)	c(25)	c(25)	c(22)							
3rd MAC	Input	x(-21)	x(-22)	x(-23)	x(-24)	x(-25)	x(-26)	x(-27)	x(-28)		3rd MAC	Input	(71-)x	x(-18)	(61-)x	x(-20)	x(-21)	x(-22)	x(-23)	x(-24)	
1st MAC	Input	c(28)		1st MAC	Input	c(24)	c(24)	c(24)	c(24)	c(24)	c(24)	c(24)	c(24)								
MAC		2311: y(7)	2312: y(6)	2313: v(5)	2314: y(4)	2321: v(3)	2322: v(2)	2323: v(1)	2324: y(0)		MAC	2	2311: v(7).	2312: v(6)	2313: y(5)	2314: y(4)	2321: y(3)	2322: v(2)	2323: v(1)	2324: y(0)	

Computation Cycle N

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CUITIDUIATION CYCLE IN+2	3rd MAC 2nd MAC 4	nput Input Input Input Input Input	x(-14) 2331: y(7) c(22) x(-15) c(23)	(21) x(-15) 2332: y(6) c(22) x(-16) c(23) x(-17)	(21) x(-16) 2333: y(5) c(22) x(-17) c(23) x(-18)	x(-17) 2334; y(4) c(22) x(-18) c(23)	(21) x(-18) 2341: y(3) c(22) x(-19) c(23) x(-20)	x(-19) 2342: y(2)	(21) x(-20) 2343: y(1) c(22) x(-21) c(23) x(-22)	21) x(-21) 2344: y(0) c(22) x(-22) c(23) x(-23)
Co	2nd MAC 4ti	Input	c(21) ×	c(21) x	c(21) x	c(21) x	c(21) x	c(21) x	c(21) x	c(21) x
	MAC 2nd	ndt In	x(-13) c(2	x(-14) c(2	x(-15) c(2	x(-16) c(2	x(-17) c(2	x(-18) c(2	x(-19) c(Z	x(-20) c(2
	1st MAC 3rd	Input Ir	c(20) x(	c(20) x(	c(20) x(	┝	c(20) x(	c(20) x(	c(20) x(	c(20) x(
	MAC		2311: y(7)	2312: y(6)	2313: y(5)	2314: y(4)	2321: y(3)	2322: y(2)	2323: y(1)	2324: y(0)

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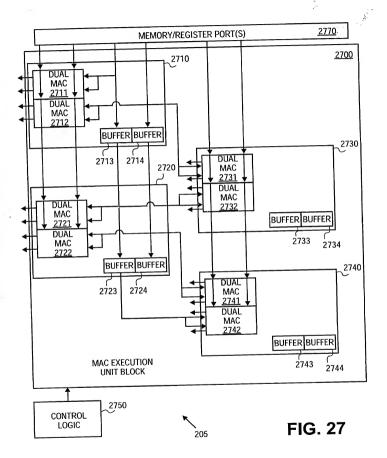
# TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062,143

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FIG. 26

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	4th MAC	Input	x(-25)	x(-27)	x(-29)	x(-31)		4th MAC	Input	x(-21)	x(-23)	x(-25)	x(-27)		4th MAC	Input	x(-17)	x(-19)	x(-21)	x(-23)
	2nd MAC	Input	c(31)	c(31)	c(31)	c(31)		3rd MAC 2nd MAC 4th MAC	Input	c(27)	c(27)	c(27)	c(27)		2nd MAC	Input	c(23)	c(23)	c(23)	c(23)
	3rd MAC 2nd MAC 4th MAC	Input	x(-24)	x(-26)	x(-28)	x(-30)		3rd MAC	Input	x(-20)	x(-22)	x(-24)	x(-26)		3rd MAC 2nd MAC 4th MAC	Input	x(-16)	x(-18)	x(-20)	x(-22)
	1st MAC	Input	(0E)0	c(30)	c(30)	c(30)		1st MAC	Input	c(3e)	(9Z)o	(52)	c(5e)		1st MAC	Input	c(22)	c(22)	c(22)	c(23)
Computation Cycle N	MAC		2531: y(6)	2532: y(4)	2541: y(2)	2542: y(0)	Computation Cycle N+1	MAC		2531: y(6)	2532: y(4)	2541: y(2)	2542: y(0)	Computation Cycle N+2	MAC		2531: y(6)	2532: y(4)	2541: y(2)	2542: y(0)
Computal	4th MAC	Input	x(-23)	x(-25)	x(-27)	x(-29)	Computation	4th MAC	Input	(61-)x	x(-21)	x(-23)	x(-25)	Computati	4th MAC	Input	x(-15)	x(-17)	(61-)x	x(-21)
	2nd MAC	Input	c(29)	c(29)	c(29)	c(29)		3rd MAC 2nd MAC 4th MAC	Input	c(22)	c(25)	c(25)	c(25)		3rd MAC 2nd MAC 4th MAC	Input	c(21)	c(21)	c(21)	c(21)
	3rd MAC 2nd MAC 4th MAC	Input	x(-22)	x(-24)	x(-26)	x(-28)		3rd MAC	Input	(81-)x	x(-20)	x(-22)	x(-24)		3rd MAC	Input	(+1-)x	x(-16)	(81-)x	x(-20)
	1st MAC	Input	c(28)	c(28)	c(28)	c(28)		1st MAC	Input	c(24)	c(24)	c(24)	c(24)		1st MAC	Input	c(20)	c(20)	c(50)	c(20)
	MAC		2511: y(6)	2512: y(4)	2521: y(2)	2522: y(0)		MAC		2511: y(6)	2512: y(4)	2521: y(2)	2522: y(0)		MAC		2511: y(6)	2512: y(4)	2521: y(2)	2522: y(0)

#### S/N: 10/062,143



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# TITLE: MULTIPLY-ACCUMULATE ACCELERATOR WITH DATA RE-USE INVENTOR(S): GAD S. SHEAFFER S/N: 10/062,143

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	4th MAC	Input	x(-20)		x(-21)		x(-22)		x(-23)			4th MAC	Input	x(-18)		x(-19)		x(-20)		x(-21)		_
	3rd MAC 2nd MAC 4th MAC	Input	c(31)		c(31)		c(31)		c(31)			2nd MAC	Input	c(27)		c(27)		c(27)		c(27)		
	3rd MAC	Input		x(-20)		x(-21)		x(-22)		x(-23)		1st MAC   3rd MAC   2nd MAC   4th MAC	Input		(81-)x		(61-)x		x(-20)		x(-21)	
	1st MAC	Input		(0E)၁		(0E)၁		(0E)၁		(0E)၁		1st MAC	Input		c(26)		c(56)		c(56)		c(26)	
Se N	C		y(7)	)(e)	y(5)	y(4)	y(3)	y(2)	y(1)	y(0)	e N+1	C		y(7)	y(6)	y(5)	y(4)	y(3)	y(2)	y(1)	y(0)	
ion Cy	MAC		2731		2732		2741		2742		on Cycl	MAC		2731		2732		2741		2742		
Computation Cycle N	4th MAC	Input	x(-19)		x(-20)		x(-21)		x(-22)		Computation Cycle N+1	4th MAC	Input	x(-17)		(81-)x		(61-)x		x(-20)		
	3rd MAC 2nd MAC 4th MAC	Input	c(23)		c(29)		c(29)		c(29)			1st MAC   3rd MAC   2nd MAC   4th MAC	Input	c(22)		c(25)		c(22)		c(22)		
	3rd MAC	Input		(-19)		x(-20)		x(-21)		x(-22)		3rd MAC	Input		(21-)x		(81-)x		(6L-)x		x(-20)	
	1st MAC	Input		c(28)		c(28)		c(28)		c(28)		1st MAC	Input		c(24)		c(24)		c(24)		c(24)	
	ပ		y(7)	9(9)	y(5)	y(4)	)(3)	y(2)	)(1)	<u>(</u>		ړ		y(7)	у(ө)	)(S)	)(4)	)(S)	)(Z)	(I)K	ý ()	
	MAC		2711		2712		2721		2722			MAC		2711		2712		2721		2722		

_											
'		4th MAC	ng L	x(-16)		x(-17)		x(-18)		x(-19)	
	3 N+2	2nd MAC	Input	c(23)		c(23)		c(23)		c(23)	
		1st MAC   3rd MAC   2nd MAC   4th MAC	Input		(91-)x		x(-17)		x(-18)		(-18)
		1st MAC	Input		c(22)		c(22)		c(22)		c(22)
		)		y(7)	y(6)	y(5)	y(4)	y(3)	y(2)	y(1)	y(0)
	on Cycle	MAC		2731		2732		2741		2742	
	Computation Cycle N+2	4th MAC	Input	x(-15)		(9L-)x		(71-)x		(81-)x	
		2nd MAC	Input	c(21)		c(21)		c(21)		c(21)	
		1st MAC 3rd MAC 2nd MAC 4th MAC	Input		x(-15)		x(-16)		x(-17)		x(-18)
		1st MAC	Input		c(20)		c(20)		c(20)		c(20)
		ي		(2)K	)(e)	y(5)	y(4)	y(3)	y(2)	)(I)	)(O)
)		MAC		2711		2712		2721		2722	